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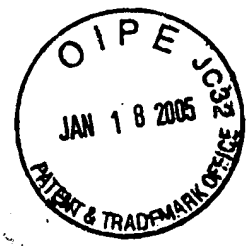

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application No:		10/657,530	Confirmation No: 9171
Applicants	:	Leland S. Swanson et al.	
Filed	:	September 8, 2003	
TC/A.U.	:	2825	
Examiner	:	Anya, Igwe U	
Docket No	:	TI-33235.1	
Customer No	:	23494	

BRIEF ON APPEAL

CERTIFICATE OF MAILING OR TRANSMISSION UNDER 37 CFR 1.8

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Jackie McBride

Jackie McBride

M. S. Appeal Brief-Patents
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In support of their appeal of the Final Rejection of claims in this application, applicants respectfully submit their brief.

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, a Delaware corporation with offices at 7839 Churchill Way, Dallas, Texas 75251.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals or interferences.

STATUS OF CLAIMS

This is an appeal of claims 33, 34, 36-39, all of the rejected claims. Claim 40 is allowed and claim 35 is conditionally allowed.

STATUS OF AMENDEMNTS

Appellants did not file an amendment in response to the final rejection of September 20, 2004.

SUMMARY OF INVENTION

The invention directs to an improved bipolar transistor. More particularly, the present invention uses a thin carbide layer and an overlying oxide layer as parts of a dielectric stack to effectively control the emitter area of a bipolar transistor.

One embodiment of the present invention describes a bipolar transistor that has a collector region **106**; a base region **112a** formed in a base layer **112** overlying the collector region **106**; an emitter-base dielectric stack **114** overlying the base layer and having an opening **124** therein exposing a portion of the base layer **112a**. The emitter-base dielectric stack comprises a carbide layer **120**; an oxide layer **116** resistive to a carbide-dry-etching process, overlying the carbide layer **120**. The bipolar transistor also has an emitter poly layer **122** overlying the emitter-base dielectric stack **114** and an exposed portion of the base layer **112a**.

The collector region **108** is described in the specification, page 14, lines 21-22; the base region is described in page 14, lines 28, and in page 15, line 6-7; the emitter-base dielectric stack **114** is described in general in page 15, line 10 to page 16, line 23; in particular, the carbide layer **120** is described in page 16, lines 3-20, and the oxide layer **116** is described in page 16, lines 21-23; the etching selectivity aspect of the oxide layer is described in page 19, lines 23-31.

ISSUE

Whether claim 33 is obvious under 35 U.S.C. 103(a) over the combination of Schuefraf (US Patent 6620732) in view of Vanhaelemeersch et al. (US Patent 6599814).

GROUPING OF CLAIMS

The claims stand and fall together.

ARGUMENTS

Issue: Whether claim 33 is obvious under 35 U.S.C. 103(a) over the combination of Schuegraf (US Patent 6620732) in view of Vanhaelemeersch et al. (US Patent 6599814).

Applicants respectfully submit that the 103(a) rejection is improper because the Office action fails to establish a prima facie case of obviousness against claim 33 for the following reasons:

1. The Office action fails to show a proper motivation in combining the references.

   It is well established that "When a rejection depends on a combination of prior art references, the PTO must show that there is some teaching, suggestion, or motivation to combine the references."[1]

   In Butler, Judge Rich reversed the decision of the Board of Patent Appeals and Interferences ("Board) of the Patent and Trademark Office ("PTO") affirming a 103 rejection. Judge Rich rejected the Board's argument that because the two cited references both are directed toward prefabricated concrete devices used in subterranean environments and the shape of the "anchor device" is a known alternative to the shape of the "footing device", it would have been obvious to substitute the shape of the anchor for the footing shape taught in the primary reference. The reason for rejecting this argument is that the two devices "serve fundamentally different purposes."

   Here, in the primary reference, Schuegraf discloses an anti-reflective

[1] In re Butler, 1999 U.S. App. LEXIS 5056 (Fed. Cir. 1999) (unpublished)

coating ("ARC") over an amorphous silicon layer; in the secondary reference, Vanhaelemeersch discloses a carbide layer (33, 43), which acts as an etch-stop to a dielectric layer (34, 44).[2] There is no requirement that the dielectric layer be resistive to the carbide dry etching process and there is no suggestion in that this dielectric layer may act as ARC.

It is well known in the art of integrated circuit manufacturing that the purpose served by ARC is fundamentally different from the purpose served by a etch mask. An ARC is used in a photographic process to reduce light reflectivity at photo-resist interfaces in order to provide linewidth control with minimal loss of photo-resist performance. As explained in the Schuegraf reference:

> The addition of ARC 346 provides a number of functions, for example, reduction of "subsurface reflection" which degrades image definition of the photoresist by exposing portions of photoresist not intended to be exposed.[3]

The "process window" of an ARC depends on how well it damps the reflections from the photo-resist interfaces, not necessarily on its etching selectivity.

Because there is nothing in the Schuegraf reference to suggest that an ARC should be resistive to the etching of the underlying layer, and there is nothing in the Vanhaelemeersch reference to suggest that the dielectric layer may act as ARC or should be resistive to carbide etch, the cited art does not suggest the desirability of creating an ARC that is resistive to a carbide etching process.

2. The combination of the references would render the prior art reference inoperable for its intended purpose.

It is also well established that a proposed modification is "inappropriate for an obviousness inquiry when the modification rendered the prior art

[2] See, US 6,620,732, col. 10, l. 62 – col. 11, l.5.
[3] Ibid, col. 6, ll. 15-19.

reference inoperable for its intended purpose.[4]

The Schuegraf discloses a polycrystalline silicon emitter structure and the method for controlling its critical dimension. The method includes a step 276 – selectively etch anti-reflective coating and amorphous silicon layer without etching underlying etch stop layer. The detail embodiment of this step is copied below:

> ...step 276 of flowchart 200 comprises selectively *etching ARC 346 and amorphous silicon layer 344* of structure 374. The purpose of etching is to open a "window" onto top surface 324 of base 320. The window will allow for subsequent formation of an emitter comprised of N-type polycrystalline silicon on top surface 324 of base 320. The etching is done selectively, i.e. etchants are used which etch silicon oxynitride ARC 346 and amorphous silicon layer 344 but do not substantially etch silicon dioxide etch stop layer 342. Suitable etchants with the desired properties are known in the art. For example, etchants that could be used include CF_4 and chlorine compounds known in the art.[5] (emphasis added)

It is clear from this passage that Schuegraf intended to use a one-step etch to open a window through the ARC and the amorphous silicon layer. The choice CF_4 for etching amorphous silicon and silicon oxynitride makes the one-step etching possible. To substitute the carbide-etching resistive oxide layer for the oxynitride layer (even though the references do not suggest it) would achieve the diametrical result – the oxide layer and the carbide layer must be etched separately and, therefore, the process of a one-step etching will be inoperable.

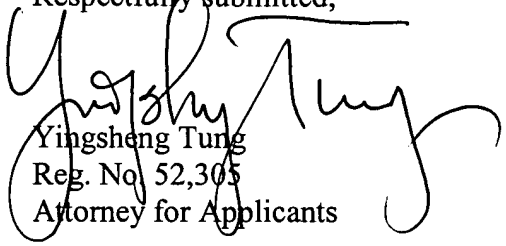
Conclusion

Because the cited references in the Office action do not suggest combining the references and because the proposed combination in the Office action would render the reference inoperable for its intended purpose, the final Office action fails to establish

[4] In re Fritch, 972 F.2d. 1260, 23 U.S.P.Q. 2d 1780 (Fed. Cir. 1992)
[5] US 6,620,732, col. 6, l. 56 – col. 7, l. 1.

prima facie case of obviousness and therefore improperly rejects claim 33 under 35 U.S.C. 103(a). Applicants respectfully request the Board to reverse the final rejection and allow the claim 33 and its dependent claims on appeal.

Respectfully submitted,



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APPENDIX

The claims on appeal read as follows:

33. A bipolar transistor, comprising:

a collector region;

a base region formed in a base layer overlying the collector region;

an emitter-base dielectric stack overlying the base layer and having an opening therein exposing a portion of the base layer, the emitter-base dielectric stack comprising a carbide layer;

an oxide layer resistive to a carbide-dry-etching process, overlying the carbide layer; and

an emitter poly layer overlying the emitter-base dielectric stack and an exposed portion of the base layer.

34. The transistor of claim 33, wherein the emitter-base dielectric stack comprises:

a first oxide layer overlying the base region of the base layer; and

the carbide layer overlying the first oxide layer.

36. The transistor of claim 34, wherein the first oxide layer comprises a first silicon oxide overlying the base layer and having a thickness between about 70 Å and about 100 Å.

37. The transistor of claim 34, wherein the carbide layer comprises a silicon carbide layer overlying the first oxide layer.

38. The transistor of claim 37, wherein the thickness of the silicon carbide layer is about 100 Å.

39. (currently amended) The transistor of claim 37, wherein the second oxide layer comprises a second silicon oxide overlying the carbide layer and having a thickness between about 500 Å and about 1000 Å.